A 0.18μm FOUNDRY RF CMOS TECHNOLOGY WITH 70GHz FT FOR SINGLE CHIP SYSTEM SOLUTIONS

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Abstract **- This paper presents a high performance RFCMOS technology with a complete portfolio of RF and base band components for single-chip systems. Using optimized CMOS topology and deep n-well, we obtain a F_t of 60GHz and F_{max} of 55GHz at 10mA, a F_t of 70GHz and F_{max} of 58GHz at maximum-transconductance bias, and a minimum noise figure of 1.5dB without ground-shielded signal pad. High quality-factor inductors are obtained using Copper interconnect giving a quality factor of 18 at 1.7nH. MIM capacitors, as well as accumulation and junction varactors are also optimized for enhancing quality factor. For the purpose of eliminating inter-block coupling noise penetrating through substrate, a deep n-well isolation and p-ring have been adopted to suppress the substrate noise by 25dB and 10dB respectively. This technology provides a complete solution for single-chip wireless systems.**

I. INTRODUCTION

In the development of short-range wireless communications, CMOS has received tremendous interest in its integration with high performance digital circuits and high-speed analog circuits [1][2]. However, there exist several major issues of adopting CMOS for RF products such as (1) The RF performance of MOS itself has been a bottleneck due to its limited F_t, F_{max}, and noise performance reported [3]; (2) The availability of RF passive components, as the fine-pitch and thin-line metallization approach physically conflicts with the requirement of high-quality-factor (Q) and low loss; (3) In addition, the coupling noise propagation through the substrate degrades the feasibility of integrating digital, analog and RF blocks on the same chip [4, 5], such as the noise generated during CMOS digital switching.

In this paper, we present a RF CMOS technology capable of making an integrated system. CMOS cells with optimized F_t, F_{max} and noise-figure have been obtained by using a deep n-well implantation and an optimized topology. High-Q inductor has been developed using 2 μm AlCu top-level metal, and optimized at several application-specific frequency bands. Substrate coupling noise has been suppressed by the deep n-well and light-p-ring isolation. These features provide a complete solution for the above-mentioned concerns for using CMOS technology to implement RF circuits and single-chip RF systems.

II. OPTIMIZING RF MOS

The CMOS performance has been optimized for F_t and F_{max} through device engineering and a proper selection of finger width W_f as shown in Fig. 1. As shown in Fig. 2(a) and (b), we obtained optimized peak F_t and F_{max} of 70GHz and 58GHz respectively using W_f=10μm and with underneath deep n-well. The deep n-well de-couples the substrate and associated signal loss from the NMOS through the junction capacitor, hence enhances power gain at frequencies above 0.9GHz. The noise figure of this RF MOS cell is shown in Fig. 3, giving a NF_{min} of 1.5dB at 1.8GHz without ground-shielded signal pads. The maximum stable power gain performance of this RF MOS cell is shown in Fig. 4, which are comparable to 0.35μm silicon BiCMOS at around 2mA[5].

II. HIGH-Q PASSIVE COMPONENTS

In this technology, high-Q inductors can be formed using the top AlCu metallization layer of thickness 2 μm without added mask. In inductor optimization, the frequency for peak quality factor (Q) is very important, due to the fact that high Q value is only needed at specifically the operation band, with commonly used bands include GSM (0.9 and 1.8GHz), and Bluetooth (2.4GHz). Based on this scenario, we developed an inductor layout optimization algorithm in order to optimize its Q value at the above-mentioned frequency bands for a wide range of inductance. Our algorithm is based on a global tradeoff between resistive loss and substrate-induced self-resonance effects, as well as an analytical estimation of target inductance values. The results of our inductor layout optimization at specified frequency bands are shown in Fig. 5, with the peak-Q value obtained at 1.9GHz and 2.4GHz for the inductance

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of 1.5nH and 4.1nH respectively. The inductor performance, in terms of quality factor, can be further enhanced using the Copper top-wiring layer of 2.8 μm thickness. The Cu inductor gives, for a 1.7nH inductor, a peak Q of 18 at 4.8GHz and Q of 14 at 2.4GHz as shown in Fig. 6, which is superior than the work in [7,8]. The peak Q in the work of [7] and [8] was 14 and 16 with similar inductance, respectively.

A MIM capacitor of 1fF/μm^2 has been developed using oxide inter-metal dielectric, giving voltage coefficient of 60ppm/V, temperature coefficient of 50ppm/^oC, and Q of 100 and 40 at 2.4GHz and 5.3GHz respectively at 1.1pF as shown in Fig. 7. The small via-5 resistance on the capacitor top plate allows for good Q value.

IV. Integrated Varactors

Both accumulation-mode (using 32 angstrom gate oxide) and P+ N junction varactors are provided, giving sharp-transition and tapered transition in the C-V tuning range respectively. As shown in Fig. 8(a) and Fig. 8(b), the accumulation mode varactor gives a tuning range of 50% with an optimized Q of 18 at 2.4GHz, better than published results with similar capacitance range [9]. The P+N junction gives 55% tuning range with Q of 50 at 2.4GHz for 1.5pF as shown in Fig. 9(a) and Fig. 9(b), respectively. The junction varactor gives higher Q than the accumulation varactor due to the low resistance of Cobalt silicided diffusion layers. These varactors can be used for VCO to achieve good phase noise performance.

V. Substrate Coupling Noise Surpression

A critical issue in system integration is the substrate coupling noise [4], which could be induced by digital circuits disturbing small-signal analog circuits, or induced by a large-signal RF circuit (such as an oscillator) disturbing a small-signal circuit (such as a LNA). This noise propagation is more pronounced in standard CMOS technology using low-resistivity substrate. High resistivity substrate, though capable of improving coupling noise as well as reducing component signal loss [10], may induce serious latch-up problems. In this technology, we adopt the deep n-well as a noise stopper. As shown in Fig. 10(a), with a p+ diffusion representing a noise injector, the deep n-well can be placed surrounding the p+ injector and biased through a surface n-well connected to the deep n-well. The received noise power is measured from another p+ diffusion, namely the noise receiver, using a network analyzer. As shown in Fig. 10(b), the coupled noise measured from the receiver can be improved by 40dB at 1MHz and improved by 25dB at 2.4GHz. This demonstrates that placing a deep n-well surrounding the noisy circuits can successfully eliminate the coupled noise to other sensitive circuits. It should be noted in Fig. 10(c) that, although increasing the inter-P+ spacing also reduces the injected noise, the amount of noise power reduction is only around 5dB per 50μm spacing increase, being significantly inferior to the effect of applying a deep n-well.

VI. Manufacturability Of Rf Circuits

The manufacturability of this RF CMOS technology has been verified using a voltage controlled oscillator (VCO). This VCO uses an accumulation-mode MOS varactor, RFCMOS cell of 90μm channel width and a 3nH AlCu inductor. As shown in Fig. 11, the VCO performance shows only 4% process fluctuation over than 1000 samples from 3 lots, on oscillation frequency. This tight fluctuation can be attributed to the small deviation of inductance and varactor capacitance in LC tank.

VII. Conclusion

A 0.18μm foundry RF CMOS technology has been presented, including all desired RF, analog and digital components. We provide integrated passives components with good Q value, and system-integration solution including substrate coupling noise suppression. The manufacturability of this RFCMOS has been verified through a VCO, which gives 4% frequency fluctuation over 3 lots.

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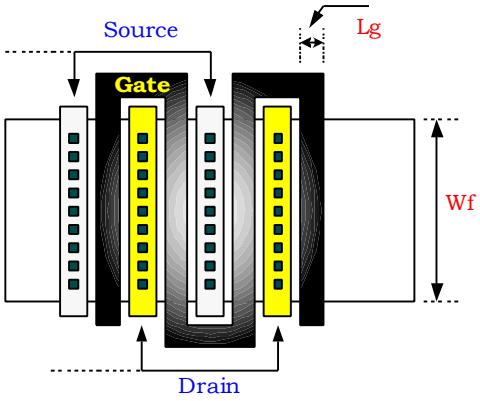

Fig. 1 Top view of RF MOSFET layout.

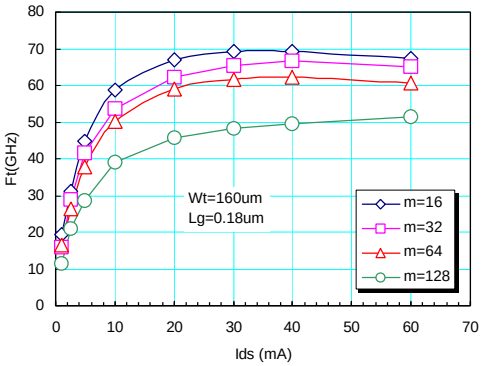

Fig. 2(a) Cut-off frequencies of n-type MOSFET with finger-number optimization.

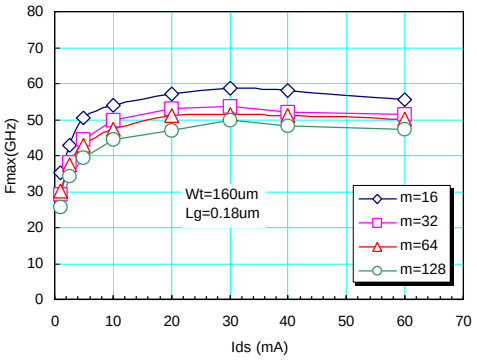

Fig. 2(b) Maximum oscillation frequency of n-type MOSFET with finger number optimization.

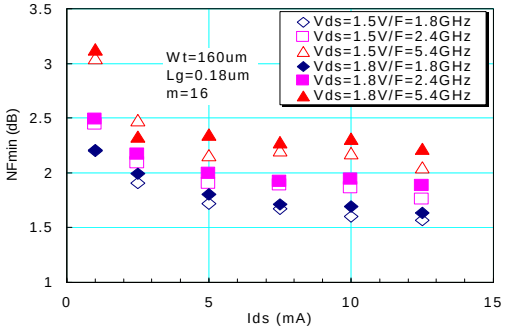

Fig. 3 NFmin versus Ids plot with various frequencies.

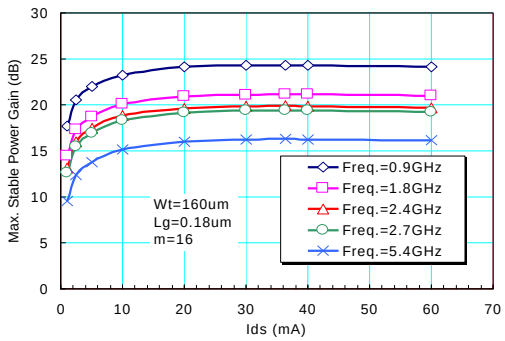

Fig. 4 Maximum stable power gain of MOS.

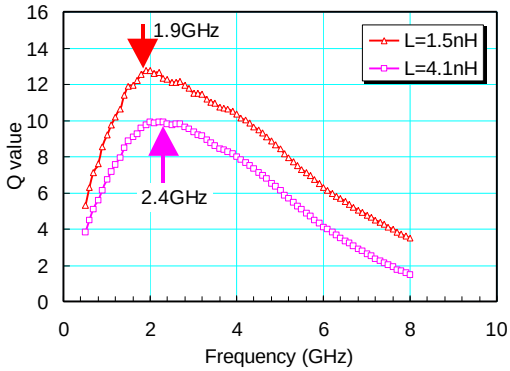

Fig. 5 Peak-Q value inductor optimization at specified frequency.

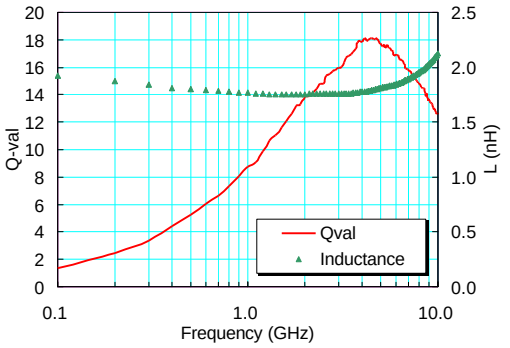

Fig. 6 Q value and inductance of 2.8μm Cu inductor.

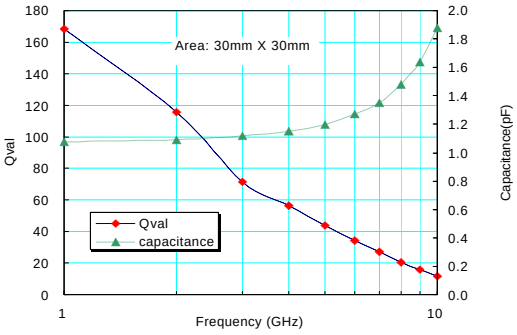

Fig. 7 Q value and capacitance of MIM capacitor.

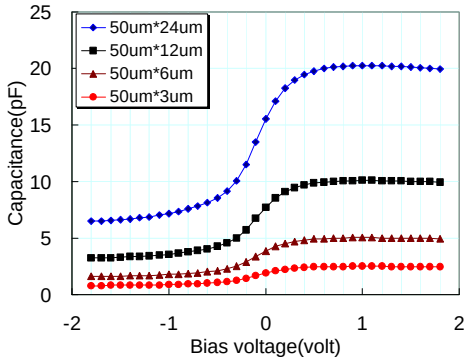

Fig. 8(a) Tuning range of accumulation mode MOS varactor.

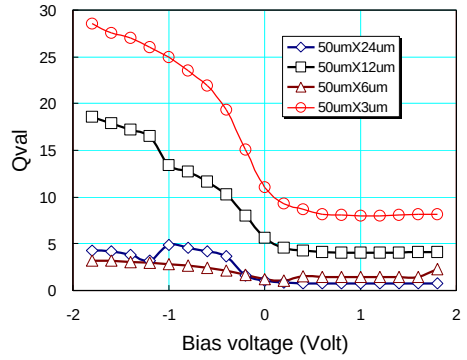

Fig. 8(b) Q value of accumulation mode MOS varactor.

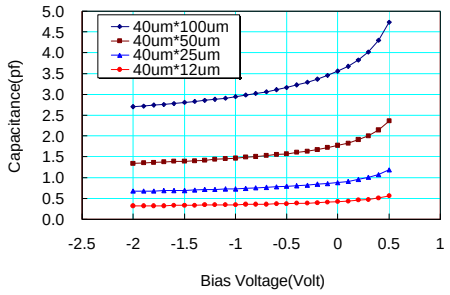

Fig. 9(a) Tuning range of junction varactor.

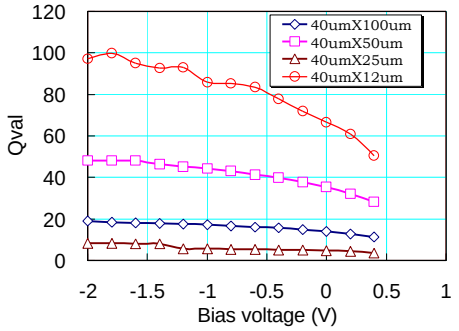

Fig. 9(b) Q value of junction varactor.

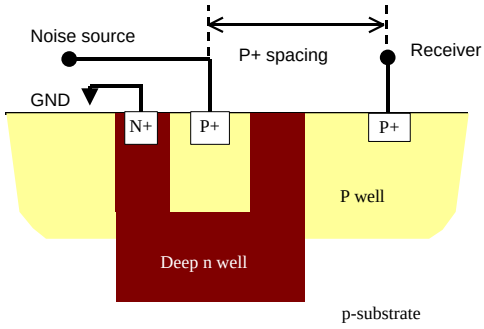

Fig. 10(a) Schematic of substrate coupling noise experiment.

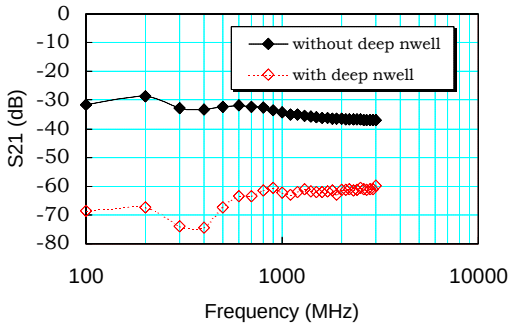

Fig. 10(b) Substrate coupling noise suppressed by using deep n-well structure.

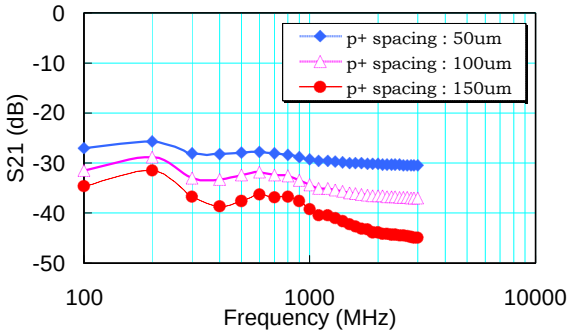

Fig. 10(c) Substrate coupling noise with different p+ spacing.

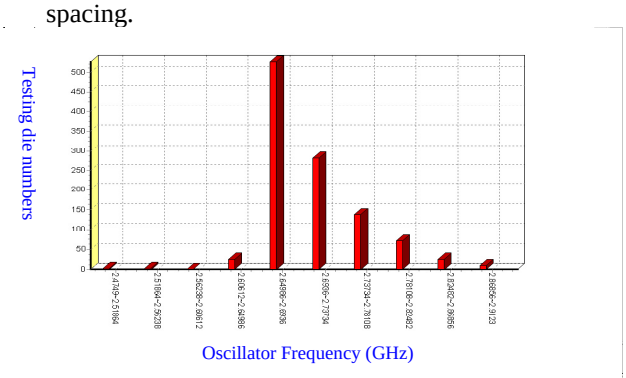

Fig. 11 The histogram plot of VCO oscillator frequency.